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EXAMINER	
TRUJILLO, JAMES K	
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

85

Office Action Summary	Application No. 09/657,255	Applicant(s) SITA ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Amendment A dated 11/19/03.

2. Claims 1-17 and 19-24 are presented for examination. The applicants have canceled claim 18.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 13, 19, 21 and 23 are objected to because of the following informalities:

a. As to claim 13, claim 13 has not been amended as per previous Office Action in the claims. However, comments in the remarks suggest that it should have been changed as per the suggested language in the last Office Action.

b. As to claim 19, on line of claim 1, "19" should be changed to "20" due of a minor oversight because claim 19 cannot be dependent upon itself. For purposes of examination it will be assumed as such.

c. As to claim 21, on line 10 of the claim, "coupled an" should be "coupled to an" for clarity.

d. As to claim 23, on line 11 of the claim, "Iatching" should be changed to "latching". Appropriate correction is required.

5. Applicant's arguments with respect to claim 1-17 and 19-20 have been considered but are moot in view of the new ground(s) of rejection.

6. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hassoun, U.S. Patent 6,487,648 (cited in last office action).

7. Claim 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hassoun et al., U.S. Patent 6,587,534.

8. As to claim 1, Hassoun taught, as per claim 1, a method comprising the steps of:

a. receiving a first clock (CLK_FB) [figure 5];

b. providing a distributed clock signal (CLK_SD) to a clock distribution network having a plurality of endpoints (CLK_SD is distributed to different memory devices) connected to a respective plurality of components (SDRAM 308 and 309) [figure 5]; and

c. modifying the distributed clock signal (by Delay Lock Loop 304) until a portion of the distributed clock signal received at the first end of the plurality of endpoints point (CLK_SD at the input to SDRAMS 308 and 309) is substantially synchronized to the first clock signal (the first clock and distributed clock signals are substantially synchronized because they are at the same node) [figures 4 and 5].

9. As to claim 2, Hassoun taught the method according to claim 1 described above. Hassoun further taught wherein the step of modifying includes providing a delayed representation (delaying using a delay line and a clock phase shifter of the DLL) of the distributed clock signal at the first endpoint [col. 10 lines 5-14 and col. 10 lines 34-59].

10. As to claim 3, Hassoun taught the method according to claim 2 described above. Hassoun further taught wherein the step of modifying includes using a delay locked loop (DLL 304) to modify the distributed signal [figure 5].

11. As to claim 4, Hassoun taught the method according to claim 3, described above. Hassoun further taught wherein the first endpoint (input to SDRAMS) is at the same propagation level as a second endpoint (input to the DLL 304) of the clock distribution network, where the second endpoint drives a component (DLL 304) that is not part of the clock distribution network and the first endpoint drives an input to the delay lock loop [figure 5]. Essentially, Hassoun has the DLL connected to endpoint (node) that is connected to the first endpoint. This second endpoint of Hassoun has the same propagation level because it is at the same node as the first endpoint.

12. As to claim 5, Hassoun taught the method according to claim 4, described above. Hassoun further taught providing a second clock signal (O_CLK to the clock skew 502) from a first device (the first device is the DLL at the output) wherein the first clock signal is a delay representation (because of clock skew) of the second clock signal [figures 3 and 4].

13. As to claim 6, Hassoun taught the method according to claim 5, described above. Hassoun further taught wherein the step of providing the second clock signal includes providing the second clock signal to a propagation path manufactured onto a first substrate (off of the substrate of the controller core and PLD where clock skew is incorporated), wherein the first substrate is not part of the first device [figure 3-5]. Hassoun discloses, in figures 3-5, that O_CLK originates from a first device and is sent off the device. Figure 3 clearly suggests that the clock skew must be a separate device from the first device and therefore must have its own substrate. Because the first device is on the PLD, the first substrate (depicted as having clock skew) cannot be part of the first device.

14. As to claim 7, Hassoun taught the method according to claim 6, described hereinabove. Hassoun further taught wherein the step of receiving the first clock signal (CLK_FB) includes receiving the first clock signal at the first device (the DLL) [figure 5].

15. As to claim 8, Hassoun taught the method according to claim 5, described above. Hassoun further taught wherein the step of receiving the first clock signal (CLK_FB) includes receiving the first clock signal at the first device (the DLL) [figure 5].

16. As to claim 9, Hassoun taught the method according to claim 3, described above. Hassoun further taught providing a second clock signal (O_CLK to the clock skew 502) from a first device (the first device is the DLL at the output) wherein the first clock signal is a delay representation (because of clock skew) of the second clock signal [figures 3 and 4].

17. As to claim 10, Hassoun taught the method according to claim 9, described above. Hassoun further taught wherein the step of providing the second clock signal includes providing the second clock signal to a propagation path manufactured onto a first substrate (off of the substrate of the controller core and PLD where clock skew is incorporated), wherein the first substrate is not part of the first device [figure 3-5]. Hassoun discloses, in figures 3-5, that O_CLK originates from a first device and is sent off the device. Figure 3 clearly suggests that the clock skew must be a separate device from the first device and therefore must have its own substrate. Because the first device is on the PLD, the first substrate (depicted as having clock skew) cannot be part of the first device.

18. As to claim 11, Hassoun taught the method according to claim 10, described above. Hassoun further taught wherein the step of receiving the first clock signal (CLK_FB) includes receiving the first clock signal at the first device (the DLL) [figure 5].

19. As to claim 12, Hassoun taught the method according to claim 9, described above. Hassoun further taught wherein the step of receiving the first clock signal (CLK_FB) includes receiving the first clock signal at the first device (the DLL) [figure 5].

20. As to claim 13, Hassoun taught the method comprising the steps of:

a. providing a first clock signal from a first device (from Delay Lock Loop (DLL) 300 at terminal 304) [figure 3].

b. receiving a representation of the first clock signal from a device external to the first device at the first device (from clock skew 180 at terminal 306, clock skew is caused by various devices not shown) [figure 3, col. 1 lines 55 through col. 2 line 4 and col. 5 line 24-49];

c. providing the representation of the first clock signal to a delay element (delay element such as clock buffers, not explicitly shown but suggested as existing in clock skew 180) [figures 1 and 3, col. 1 lines 55 through col. 2 line 4 and col. 5 line 24-49];

d. providing a delayed clock signal from the delay element to a clock distribution tree (S_CLK is provided to a plurality of logic circuits 190, this interpreted to be a clock distribution tree), wherein the delay clock signal is based upon the representation of the first clock signal (it is based upon the clock signal from DLL 300), and the clock distribution tree includes a plurality of leaves that provide the delay clock signal to a respective plurality of components (the leaves and components are the logic circuits of Hassoun) [figures 1 and 3, col. 1 lines 55 through col. 2 line 4 and col. 5 line 24-49];

e. providing a representation (clock skew containing delay from a group of devices and elements including representation of all the leaves) of the delayed clock signal (at terminal 306) from the leaves (wherein a leaf is interpreted to one of the logic circuits 190) to the delay element (wherein the leaves are the logic circuits); and

f. modifying the delayed clock signal (by DLL 300) provided by the delay elements based upon the representation of the delayed clock signal (at terminal 306) [figure 3 and col. 5 lines 24-49].

Hassoun does not expressly disclose providing a representation of the delay clock from *a first leaf* to the delay element wherein the *first leaf is one of the plurality of leaves* and wherein the modification is made base on *the first leaf*. Hassoun instead discloses wherein the delay caused by a plurality of leaves (delays in various clock buffers and propagation delays on the clock signal line) as a single lumped clock delay (clock skew 180) [col. 1 line 55 through col. 2 line 4]. Hassoun uses this model to simplify the analysis. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hassoun by separating the delays into a plurality of leaves (as a plurality of clock skews). An artisan would have been motivated to do so to model the effect of each delay individually rather than all the delays as a whole.

21. As to claim 14, Hassoun taught the method according to claim 13 described above. Hassoun does not expressly disclose wherein the step of modifying the delayed clock includes modifying the delay by delaying the first clock by an amount approximately equal to a first propagation delay *and a second propagation delay*, wherein the *first propagation delay* is equal

to a delay along a path *from the first device to a second device*, and the *second propagation delay* is equal to a delay along a delay path *from the second device to the first device* [emphasis added].

However, Hassoun teaches a first delay modeled as skew 180. The delay is incorporated in a feedback path from the output (304) of first device back to an input (306) of the first device (DLL 300). Hassoun teaches that the delay is a model of the delay of various devices. Specifically, Hassoun discloses that the delay is from various clock buffers and delays on the clock line [figures 1, 3, 10 and col. 1 lines 15-45, col. 5 lines 23-49 and col. 11 lines 26-47]. Essentially the only difference between Hassoun and the claimed invention is the number of device in a feedback loop. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hassoun by modeling the delay (skew 180) as a the propagation delay in the path from the first device (DLL 300) to the single second device and from likewise back from the second device to the first device (DLL 300). An artisan would have been motivated to do so in order to model a single device rather than a plurality of devices thereby accounting for a specific desired device in an environment with only one device in the feedback loop..

22. Claims 15-17 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, U.S. Patent 6,003,118.

23. As to claim 15, Chen teaches a method comprising the steps of:

a. generating a first clock edge (at 224) at a first device (memory controller) at a first time, wherein the first clock edge is associated with a first clock having a first clock period [figures 2A and 3];

b. receiving the first clock edge (at 234) at a second device (memory module) at a second time, wherein the time between the first time and second time is a first propagation delay [figures 2A and 3];

c. generating a data signal (at 238) at the second device at a third time in response to receiving the first clock edge, wherein the time between the second time and the third time is a second propagation delay [figures 2A and 3];

d. receiving the data signal at a first component of the first device at a fourth time (at 244), wherein the time between the third time and the fourth time is a third propagation delay (T_{ACCESS}) [figures 2A and 3];

e. providing a representation of the first clock to a delay component (load 256 providing load to cause a delay), wherein the representation of the first clock is approximately equal to the first clock delayed by an amount approximately equal to the sum of the first, second and third delays (phase lead and phase lag compensate for phase difference between clock signals at memory module, read data buffer and write buffer due to different paths) [figures 2A, 3, col. 4 lines 31-39 and col. 8 lines 15-21];

f. generating a distributed clock from the delay component (PLL in combination with load 256) to drive a clock distribution network having a plurality of endpoints [figure 2B and col. 4 lines 18-19]; and

g. receiving at the delay component a representation of the distributed clock at a first endpoint of the plurality of endpoints [figure 2B col. 4 lines 31-39]; and

h. modifying the distributed clock until the representation of the distributed clock at the first endpoint is synchronized with the representation of the first clock (using PLL 220) [figure 2B].

Chen does not expressly disclose providing a representation of the first clock to a *delay component of the first device*, wherein the representation of the first clock is approximately equal to the first clock delayed by an amount approximately equal to the sum of the first, second and third delays [emphasis added].

Specifically, in the embodiment of Chen described above, Chen separates the delay component (load 256) from the first device (controller 202).

However, Chen in figure 2A also suggests using a synchronization means (23) on the first device (microcontroller 21). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chen by having the synchronization means with the delay component and clock driver for clock distribution on the microcontroller because Chen suggests doing so.

24. As to claim 16, Chen taught the method according to claim 15 described above. Chen further taught wherein the second device is a memory device (memory module 236) [figures 2A and 2B].

25. As to claim 17, Chen taught the method according to claim 15 described above. Chen does not expressly disclose wherein the first period is less than approximately 5 nanoseconds.

However, it would have been obvious to one of ordinary skill in the art to modify Chen by making the device of Chen work with clock speeds in an environment where the period is less

than approximately 5 nanoseconds. An artisan would have been motivated to do so because the signal timing in Chen is desirable in environments where the period of the clocks is less than approximately 5 nanoseconds.

26. As to claim 20, Chen taught an apparatus comprising:

a. a phase locked loop (220) having a reference input (216), a feedback input (218)and a delayed reference output (222) [figure 2B];

b. a distribution network (clock driver 230) having a first node (228) connected to the delayed reference output, and a plurality of end nodes (234 and 254) connected to a respective plurality of components, a first end node (254) of the plurality of end nodes connected to the feedback input (218) of the phase lock loop, where the phase lock loop is one of the plurality of components [figure 2B];

c. a first input port having an output node (260) coupled to the reference input (electrically coupled to 216 for phase locking) of the phase locked loop (220), and an input node (to 218), wherein the first input port and the phase lock loop are formed on a first substrate (both the phase lock loop and the first input are on microcontroller 202) [figure 2B];

d. a first trace (258) connected (connected to 218 via 260) to the input node of the first input port wherein the first trace is formed on a second substrate (not on the microcontroller therefore on a second substrate) which is different than the first substrate (off of the microcontroller) [figure 2B];

e. a first output port (224) having an output node (226) coupled to the first trace (coupled by the PLL 220), wherein the output port is formed on the first substrate (224 is part of the microcontroller).

Chen does not expressly disclose using a *delay locked loop*. Instead Chen uses a phase locked loop for synchronization.

However, one of ordinary skill in the art would have readily recognized that a phase locked loop and a delay locked loop are functionally equivalent because both are use to synchronize a reference signal to another input signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chen by utilizing a delay locked loop in place of the phase locked loop resulting in the claimed invention.

Chen does not expressly disclose wherein the distribution network is on the first substrate along with the first input port and the delay lock loop in his preferred embodiment.

However, Chen suggests in another embodiment with synchronization means (23) having the distribution network on the same microcontroller as the first input port ant the delay locked loop as depicted in figure 2A. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chen by shifting the location of the clock driver 230 to the microcontroller as suggested by Chen resulting the in the distribution network being on the first substrate resulting in the claimed invention. Furthermore, an artisan would have been motivated to place the microcontroller and the distribution network on the same device because integrating devices on the same circuit improves timing, reliability and cost.

27. As to claim 19, Chen as modified above taught the apparatus according to claim 20 described above. Chen further taught wherein the distribution network is a clock distribution network (clock driver 230) [figure 2B].

28. As to claim 21, Chen as modified above taught the apparatus according to claim 20 described above. Chen the apparatus further comprising:

a. a second output port (output of the clock driver) having an output node connected to a second trace (trace connecting clock driver and memory module), wherein the second output port is formed on the first substrate (because as modified above the output of the clock drive would be on the microcontroller) [figure 2B].

b. a second device (load 256) having an input (at 254) coupled (because CLK_L is coupled to CLK_M) to the second trace (from the clock driver) and an output coupled to a third trace (at 258) [figure 2B];

c. the first input port having an input node connected to the third trace (the third trace becomes the first trace which is connected to the input port and is thus formed on the second substrate) and an output node coupled (to load 256) to an input of one of the plurality of components.

Chen does not expressly disclose *wherein the second trace is formed on the second substrate, and wherein the second device is formed on a third substrate different from the second substrate.*

The second trace is formed outside the microcontroller connecting the clock driver to CLK_M. CLK_M is the clock for the memory module. The first trace is on the second substrate

and is connected to the load, which simulates the behavior of CLK_M at node 254 [col. 4 lines 31-39]. It would have been obvious to one of ordinary skill to modify Chen such that the second trace is on the same substrate as the first trace. One of ordinary skill would have made the modification because doing so would make the simulation of the behavior of CLK_M more accurate.

Load 256 is used to simulate the effect of the memory module. This device is different from a trace. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Chen by placing the load on a third substrate to simulate the effect of the memory module. Because the load is a device an artisan would have recognized that it should be on substrate different than the first trace to more accurately simulate the behavior of the memory module.

29. As to claim 23, Chen taught the method comprising the steps of:

a. providing a first clock signal (CLK_M) from a first device (controller 202 via the clock driver), wherein the first clock signal is transmitted over a first substrate to a second device, wherein the first substrate is not part of the first or second device (to 234) [figure 2B];

b. providing a second clock signal (CLK_L) from the first device (microcontroller via the clock driver), wherein the second clock signal is transmitted over a second substrate, wherein the second substrate is not part of the first or the second device [figure 2B];

c. receiving the second clock signal at a delay component (load 256) as a modified second clock signal (modified to simulate CLK_M) [figure 2B and col. 4 lines 31-39];

d. receiving a third signal at a storage component (238), in response to the first clock signal (at time t-T_{PADIN}-T_L+T_{ACCESS}), wherein a latching signal is based upon the modified second clock signal (based on CLK_L) and a previous latching signal (234) from the delay component (through PLL); and

e. latching the third signal at the storage component based upon the latching signal (data is latched at 244).

Chen does not expressly disclose wherein the delay component *is part of the first device* in the embodiment described. However, Chen suggests another embodiment having a synchronization means to accomplish the same result [figure 2A]. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the preferred embodiment as suggested by Chen by shifting the location of the delay component (256) and the clock driver (230) to microcontroller 202. An artisan would have made the modification because Chen suggests doing so and integrating devices on the same circuit improves timing, reliability and cost.

30. As to claim 24, Chen as modified above taught the method according to claim 23 described above. Chen further taught wherein the latching signal (signal 215 at time t + T_{PERIOD} because that is when the latching will take place for a read, col. 5 lines 51-60) is delayed from the modified second signal (254) by an amount approximately equal to a clock period of the modified second signal plus a delay time (t + T_{PERIOD} + T_{PADIN} + T_L) between the latching signal being generated and the latching signal latching the third signal [col. 5 lines 51-60 and col. 6 lines 14-20].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
January 15, 2004

THOMAS LEE
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